ANALYSIS OF AN EFFICIENT MODULAR ADDER DESIGNS BASED ON THERMOMETER & ONE-HOT ENCODING

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ABSTRACT

The key feature of theRNS benefitting modern embedded systems and the Internet-of-Thing (IoT) edge devices is its energy efficiency. Modular additionis the most important and frequent operation applied on thecomponents of RNS, including arithmetic units in the channelsas well as forward and reverse converters. The small and mediumdynamic range requirements of low-power embedded and edgedevices make the usage of the thermometer coding (TC) and one hotcoding (OHC) viable, reducing the power consumption andimproving the energy efficiency of modulo addition in comparisonto regular binary representations. Based on these techniques,
this paper presents two new energy-efficient modular adders,which, due to the carry-free internal computations, are alsohighly performing. This approach greatly simplifies themodular addition operation by eliminating the carry bitpropagation during the arithmetic operation encountered whenusing the conventional base-2 binary code data format. It alsoenables practical applications of modular arithmetic for signalprocessing algorithms in a very efficient way. Circuit forimplementing the modular arithmetic units using multiplexersand basic logic gates are also described in this paper.

INTRODUCTION

Finite Impulse Response Filter (FIR) filter is one of the widely used Digital Signal Processing (DSP)operations which interacts its input through the convolution process. In the convolution, the output isobtained by delaying and after that scaling the input sample values. That is why conventionally, multiplyand Accumulate (MAC) based technique was generally used for FIR realization. In this technique, thethroughput is N i.e. the output is available after N clock cycles (where N = filter order) [1, 2]. DistributedArithmetic (DA) in its basic form uses bit-serial technique and avoids direct multiplication [1, 2]. TheDA uses Lookup Table (LUT) for the easy access of pre-computed values. Also, compared to MACapproach the DA technique requires the number of clock pulses proportional to bit-width of input datato get the output instead of an order of the filter.

One way to increase the efficiency of modular arithmeticunits, i.e., modulo adders, subtracts, and multipliers,is by using the one-hot coding (OHC) [7]. The one-hotresidue (OHR) has been considered for designing RNS modulararithmetic circuits based on circular shifting. TheOHC circuits based on barrel shifters show a power-delayproduct (PDP) reduction of up to 85% in comparison to theconventional positional encoding, because they significantlyreduce the circuit's activity factor. RNSs based on OHChave also been used on DSP applications due to their highspeed. Alternatively, there are other types of coding,such as the thermometer coding (TC) that can be appliedto enhance the performance of RNS modular arithmetic. Thethermometer is the unary coding, in which the number of 1'scorresponds to the magnitude of the displayed number. Thismeans that the Hamming distance between numbers representedin TC has a linear relationship to its difference.This type of coding is a subclass of Gloom coding'sused in a variety of applications, including neural networksand data compression. Moreover, the TC togetherwith distributed arithmetic can lead to fast implementations ofmodular.

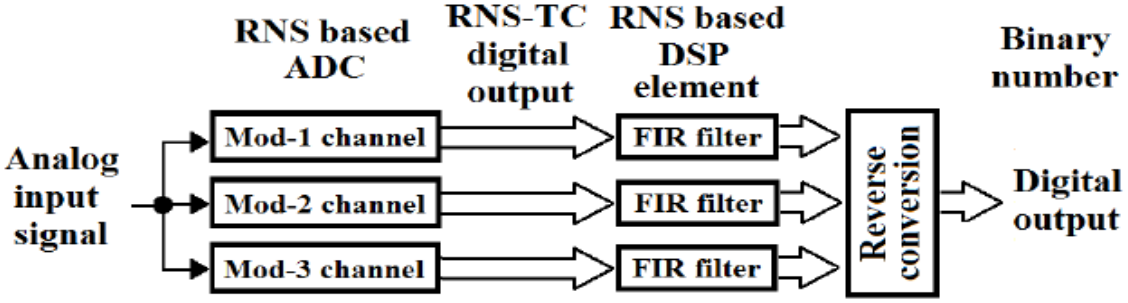

Figure 1: RNS ADC with RNS signal processing

Convention RNS representation of the residues themselvescontinue to use the base-2 BC format. In this paper, a base-1thermometer code (TC) format based RNS method is presentedto overcomes the

various limitations of the base-2 BC basedsystem as shall be described. The motivation of using the TCbased residues introduced here is also due to the availability ofa novel RNS based zero-crossing folding ADC [1] whichdirectly converts its input analog signal to digital outputs in theRNS's residues representation that are encoded in TC format asillustrated Fig. 1. Hence there is no binary to RNS forwardconversion involved in generating the RNS based data, whichis one of the main practical hindrance for RNS based signalprocessing in real world applications.

The RNS based ADC hence produces multiple channels ofresidues each encoded in TC format. Instead of convertingthese residues to conventional binary representation, it isproposed that the TC modular arithmetic operations presentedhere are used to process the TC data directly, such asperforming the digital filtering using FIR filter as shown in Fig.1, further reducing the overhead of performing the TC to BCencoding process.

It is to emphasize that the TC based method exploits thesmall dynamic range property of the residues by representingthem using the TC format where the number of bits requiredwould not be excessive and hence remains practical. Hencepractical implementation would be most feasible by usingmultiple smaller size moduli, rather than a few medium sizemoduli.

LITERATURE REVIEW

In classification analysis, the dependent variable is frequently influenced not only by ratio scale variables, but also by qualitative (nominal scale) variables. Machine Learning algorithms accept only numerical inputs, hence, it is necessary to encode these categorical variables into numerical values using encoding techniques.

This paper presents a comparative study of seven categorical variable encoding techniques to be used for classification using Artificial Neural Networks on a categorical dataset. The Car Evaluation dataset provided by UCI is used for training. Results show that the data encoded with Sum Coding and Backward Difference Coding technique give highest accuracy as compared to the data pre-processed by rest of the techniques.

This paper presents a new architecture for high-speed Finite Impulse Response (FIR) filter based onDistributed Arithmetic-Residue Number System (DA-RNS) approach. Input is represented in BinaryCode (BC) while the output is depicted using Look-up Tables (LUTs) in the proposed method. It isbeneficial to use LUTs as it avoids logic complexity due to 2k modulo factor. The Existing approachbased on shifters uses Thermometer Code (TC) and One Hot Code (OHC) respectively for input andoutput representation. Although this technique avoids the complex 2k modulo operation, the number ofinput TC bits are increased proportionally to the modulo size which results in degradation of theperformance when the actual implementation of the circuit is considered. Residue number systems (RNSs) are efficientalternatives to positional number systems, providing fast andpower-efficient computational systems. The key feature of theRNS benefitting modern embedded systems and the Internet-of-Thing (IoT) edge devices is its energy efficiency. Modularaddition is the most important and frequent operation applied on thecomponents of RNS, including arithmetic units in the channelsas well as forward and reverse converters. The small and mediumdynamic range requirements of low-power embedded and edgedevices make the usage of the thermometer coding (TC) and one hotcoding (OHC) viable, reducing the power consumption andimproving the energy efficiency of modulo addition in comparisonto regular binary representations. Based on these techniques,this paper presents two new energy-efficient modular adders,which, due to the carry-free internal computations, are alsohighly performing. The proposed modular adders based on theTC and OHC result in average improvements of 38% and 34.5%for the delay, 27% and 14.5% for the circuit area, 29.5% and6.3% for energy consumption, and about 54.9% and 44.2% forthe area-delay product (ADP), respectively, in comparison withthe related state of the art.

This paper presents a novel approach to performmodular arithmetic addition and subtraction using base-1thermometer code data format for operands corresponding to theresidues of the same modulus. Two n-bit thermometer codeoperands are first concatenated and logically shifted to produce anormalized 2n-bit thermometer code intermediate sum. Modulooperation is then applied to this 2n-bit intermediate sum toproduce an n-bit datum corresponding to the modular sum of thetwo input operands. This approach greatly simplifies the modular addition operation by eliminating the carry bitpropagation during the arithmetic operation encountered whenusing the conventional base-2 binary code data format. It alsoenables practical applications of modular arithmetic for signalprocessing algorithms in a very efficient way. Circuit forimplementing the modular arithmetic units using multiplexersand basic logic gates are also described in this paper.

3.CATEGORICAL VARIABLE ENCODING TECHNIQUES

3.1One Hot Coding

One Hot Coding is the most widelyused coding scheme. It compares each level of the categorical variable to a fixed reference level. One hot encoding transforms a single variable with n observations and d distinct values, to d binary variables with n observations each. Each

observation indicating thepresence (1) or absence (0) of the dichotomous binary variable.

3.2Ordinal Coding

In ordinal encoding, an integer is assigned to each category, provided the number of existing categories is known. It does not add any new columns to the data, but implies an order to the variable that may not actually exist. [8]

3.3Sum Coding

Sum coding compares the mean of the dependent variable for a given level to the overall mean of the dependent variable over all the levels. That is, it uses contrasts between each of the first k − 1 levels and level k in this example, level 1 is compared to all the others, level 2 to all the others, and level 3 to all the others.

3.4Helmert Coding

Helmert Coding compares each level of a categorical variable to the mean of the subsequent levels.

3.5Polynomial Coding

Polynomial coding is a form of trend analysis that looks for linear, quadratic and cubic trends in the categorical variable. This type of coding system should be used only with an ordinal variable in which the levels are equally spaced.

3.6Backward Difference Coding

In this coding system, the mean of the dependent variable for one level of the categorical variable is compared to the mean of the dependent variable for the prior adjacent level.

3.7Binary Coding

In binary coding, first the categories are encoded as ordinal, then those integersare convertedinto binary code, then the digits from that binary string are split into separate columns.

PROPOSED MODULAR ADDERS

In this section, new designs for OHR- and TCR-based modularadders are proposed. The proposed hardware structuresfor modular addition require less circuit area and less delay incomparison to the state of the art.

A. Thermometer-Based Modular Adder

An important aspect to apply the proposed method to addtwo modulo m residues($0 \leq A, B < m$) represented in TCRis to identify whether $A + B >= m$ or not. With this aim, and also for computing the sum, the order of the bits of $B$is reversed, which means the rightmost bit becomes the mostleft bit, and so on. After that, bitwise AND and NOR logicoperations are applied to the inputs A and B. If any bit of theoutput of AND gates is 1, then $A + B$ is equal to or greaterthan the modulo. More concretely, if exactly one bit of theseoutputs becomes 1, this means that $A + B = m$ and the resultshould be 0. When two bits of the outputs are 1, the resultbecomes 1, and this process is continued whenever more bitsof the output take the value 1. The outputs of the NOR gates areused to compute the result of the addition when $A + B < m$,as it will be observed in Lemma 1.*Lemma 1:* Consider two TCR numbers, A and B of m –1bits. The condition $A + B \geq m$ is verified with the bit cl, andthe result of $A + B$ *mod* m represented with $m -$ 1 bits iscomputed with the following relations:

$$\text{Sum} = \begin{cases} \text{SUM}_1, & \text{if } cl = 1 (A + B \geq m) \\ \text{SUM}_0, & \text{if } cl = 0 (A + B < m) \end{cases}$$

RNS and modular arithmetic

RNS has received varying degrees of attention from researchers in the past for implementing computer arithmetic. This number system provides a fundamental methodology for partitioning a large dynamic range system into a number of smaller but independent channels over which computations may be performed in parallel in a carry free manner between the channels. For example, using the moduli set, the decimal number X=179 will be represented using 4,3,8 residue set and the decimal number Y=254 will be represented using 2,6,2 residue set. Arithmetic operation of these two integers can be equally performed in modular arithmetic using
their residues as follows:

$$\begin{aligned} 179 \odot 254 &\cong 4,3,8 \odot 2,6,2 \\ &= 4 \odot 2, 3 \odot 6, 8 \odot 2 \end{aligned}$$

Key advantages in the modular arithmetic are twofold. Firstly is that the dynamic range (DR) of the residue set is
confined to the value of the moduli and hence is normally very much smaller compared to the decimal number that they represent. Secondly, parallel arithmetic operations can be carried out among the pairs of residues independent of each other. Both these mean that the arithmetic circuits required can be of much simpler circuitry and can be much faster when compared to conventional number addition.

Proposed DA-RNS solution

The problem of modulo 2^k factor is addressed by TCR-OHR (One hot Residue) based DA-RNS solution [2]. In this architecture, for modulo (m) TCR based computation, (m-1) bits are needed for input data representation also OHR use m bits to encode a particular digit as shown in Fig. 2 [2]. It is evident to state that if modulo size increases then it results in increased input word-length as well as OHR bits. Therefore, the proposed architecture of ref. [2] does not perform well enough for high-speed operation. In our proposed architecture, Binary Code (BC) is used to reduce the input word-length. While, the 2^k modulo factor problem which arises due to the usage of BC at the input of DA-RNS LUT is eliminated by using modulo 'power of two' LUTs. The detailed analysis is given in consequent sections.

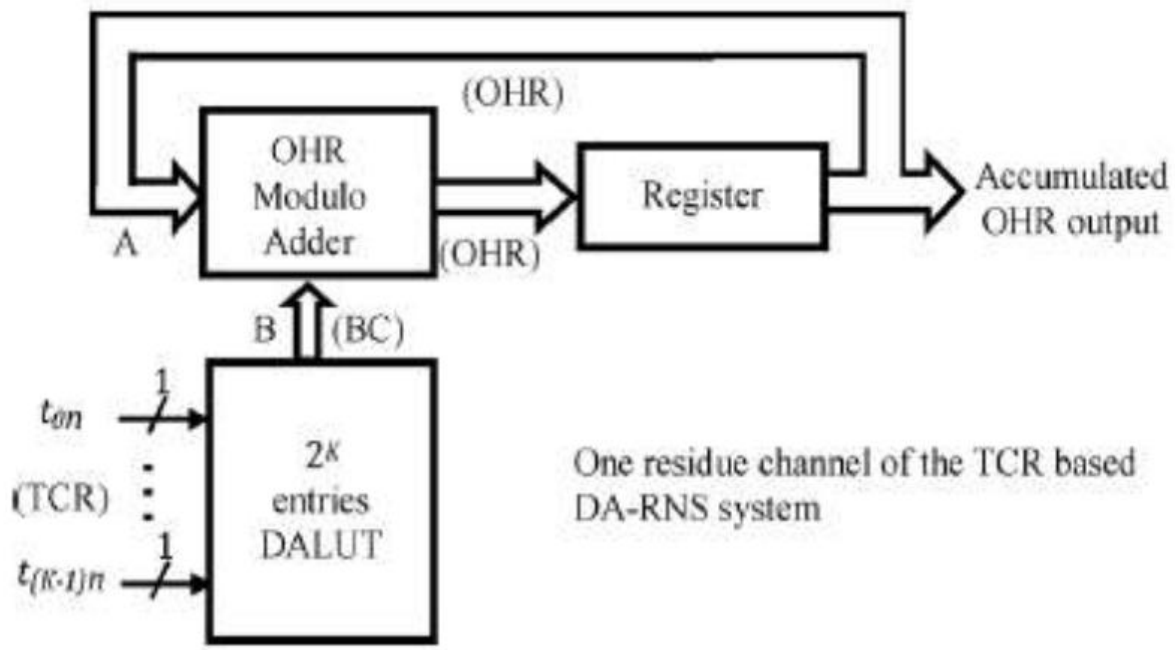

Fig. 2. One of the residue channels of the TCR based DA-RNS system for 1 BAAT operation

In Fig. 3, the architecture for high-speed FIR filter is proposed. Here, the number of ØmLUTs are required is equivalent to the input word-length used.

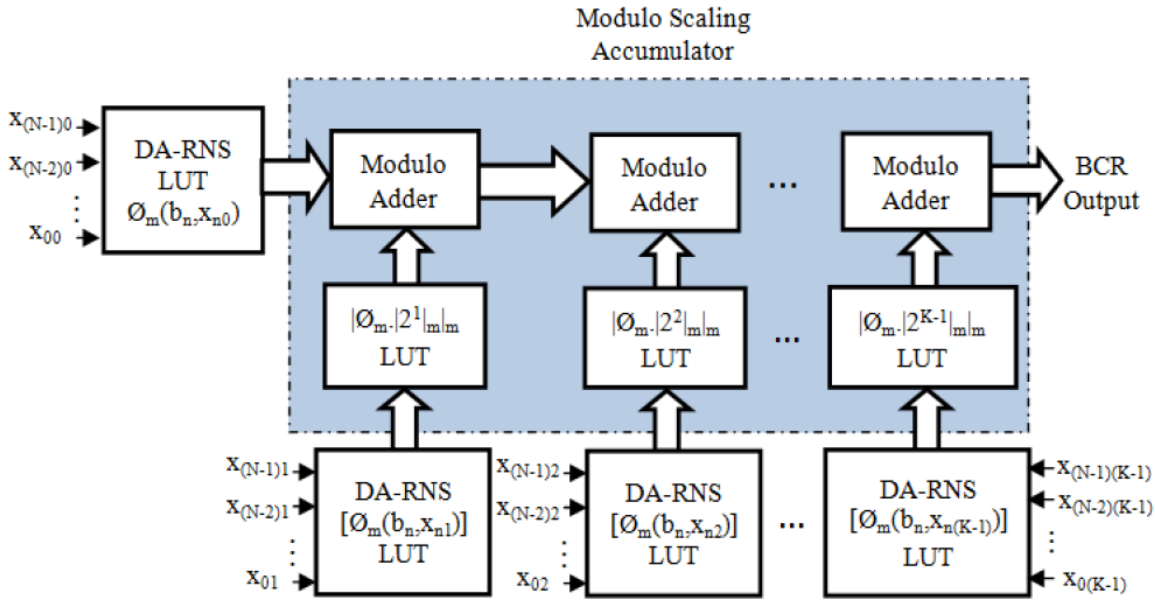

Fig. 3. Proposed high-speed architecture

CONCLUSION

In this paper, a new architecture based on DA-RNS approach is presented for high-speed FIR filter.In this architecture, the input and output is presented in binary code due to its shorter word-lengths whichresults in less hardware. The complexity of 2k modulo scaling operation involved due to the usage ofbinary codes at the input is removed by using corresponding 'power of two' LUTs. As DA basedimplementations are always based on LUTs, the inherent advantages of LUTs are maximized by usingthese at different stages of architecture. A novel thermometer code based modular arithmetictechnique has been described which provide a method toperform modular arithmetic in a highly efficient and high speedmanner. Coupled with the new RNS ADC where the output isinherently presented in RNS representation encoded in TCformat, the proposed techniques provide a mean to performsignal processing routine using the TC modular arithmeticapproach in a very efficient manner.

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